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EXAMINER	
HOYE, MICHAEL W	

ART UNIT	PAPER NUMBER
2614	15

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/398,913	KLEBANOV ET AL.	
	Examiner	Art Unit	
	Michael W. Hoye	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-13,22 and 23* is/are allowed.

6)☒ Claim(s) *14-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicants' arguments filed 3/22/04, with respect to claims 14-17, have been fully considered but they are not persuasive.

As to amended independent claim 14, the Applicants argue that, "Cheney does not appear to teach Applicants' step of "receiving a compressed transport stream . . . having data signals and control signals," and further does not appear to teach the step of "generating a secondary set of control signals from the compressed transport stream's control signals," Applicants submit that Cheney does not disclose the step of "storing at least a portion of the compressed transport stream data signals in a memory buffer controlled by the secondary set of control signals.""

In response, the Examiner respectfully disagrees with the Applicants because the Cheney et al reference discloses the claimed "receiving a compressed transport stream associated with a digital video broadcast signal" as met by the digital video from cable or satellite broadcast signal 101 (Fig. 4) received at NIM 102, where a MPEG transport stream is sent to transport logic (XPORT) 103 (see col. 6, line 35-45). The MPEG transport stream is a compressed transport stream. In addition, the claimed "compressed transport stream having data signals and control signals" is inherent to a MPEG transport stream. The Applicants also disclose this in the "Background of the Invention" (or prior art) section of the specification, which describes the Digital Video Broadcast (DVB) transmission standards and specifically states that, "The compressed MPEG 2 format is referred to as a transport stream. The transport stream from the demodulator comprises a plurality of packets. Each of the transport steam packets comprises one

synchronization byte, followed by one of 187 data bytes or 187 data bytes plus 16 extra bytes depending on the format." (See Specification, page 1, lines 15-19). Therefore, it is well known in the art that a MPEG transport stream comprises data signals as met by the data byes, and control signals as met by the synchronization bytes. The claimed "generating a secondary set of control signals from the compressed transport stream's control signals" is met by the video decode system of Figure 6, where the MPEG input source if fed through the memory control unit 652 as coded MPEG 2 video data to the input of video decoder 654 and from the decoded signals from the MPEG transport stream's control signals, the frame buffer pointer control 686 generates additional control signals (see col. 9, line 31 – col. 10, line 41). The claimed "storing at least a portion of the compressed transport stream data signals in a memory buffer controlled by the secondary set of control signals" is met by the frame buffer pointer control 686 controlling the rotation of the frame buffers (see col. 10, lines 37-41).

As to the final limitation of amended independent claim 14, the Applicants suggest that, "Adams only teaches the method of sending the contents of a memory buffer in the direction of the display and not in the direction of the system bus. As a result, Adams does not appear to disclose the step of "sending the contents of the memory buffer to a system bus" wherein the contents of the memory includes, among other things, at least a portion of the transport stream data signals."

In response, the Examiner respectfully disagrees with the Applicants because while the Adams reference teaches that the graphics display subsystem 56 is used primarily to drive the display device 12 (col. 5, lines 41-43), the Adams reference does not **only** teach a "method of sending the contents of a memory buffer in the direction of the display and not in the direction of

the system bus," but also teaches that the relationship relating to communications between the Graphics Display Subsystem 56 and the system bus 52 is bi-directional as shown in Fig. 2, where information may be communicated to other parts of the computer system, such as, the processor 52, memory subsystem 54, data modem 58, disk drive 60, etc.

As to amended dependent claim 15, the Applicants repeat the relevant remarks made above with respect to claim 14, and further argue that, "[the Cheney reference] does not appear to teach the step of "generating the secondary set of control signals from the digital video signal's control signals" and "storing at least a portion of the digital video signals in the memory buffer based on the secondary set of control signals.""

In response, the Examiner respectfully disagrees with the Applicants because of the remarks made above as related to claim 14, and in addition to, the Cheney reference also discloses another mode of operation wherein the digital video signal is of a different type than the compressed transport stream, which is met by the uncompressed digital video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67), which includes data signals including pixel data signals and control signals which are met by the corresponding synchronization signals (col. 4, lines 56-57), and by "pixel select control" signals (col. 7, lines 40-41). The digital multi-standard decoder (DMSD) 105 provides synchronization signals, such as, horizontal sync and vertical sync and the DMSD 105 provides the synchronization signals to the video decoder 106 which interprets the synchronization information and processes the data (col. 7, lines 7-18) to provide a secondary set of control signals through the use of the frame buffer pointer control 686 and other circuitry as shown in the video decode system of Fig. 6 and as previously described above in claim 14.

Applicants' arguments with respect to claims 18-20 have been considered but are moot in view of the new grounds of rejection due to the newly amended independent claim 18 language.

Applicants' arguments with respect to claim 21 have been considered but are moot in view of the new grounds of rejection.

Claim Objections

2. Claim 20 objected to because of the following informalities: There is insufficient antecedent basis for the limitation, "the system interface port," in line 2 of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Schindler et al (USPN 5,900,867), cited by the Examiner.

As to claim 18, the Schindler et al reference discloses a system for receiving a digital video broadcast signal. The claimed "tuner to receive a digital broadcast signal and to provide an analog output signal" is met by tuner 410 in Fig. 4, which receives a digital signal that is transmitted on an analog carrier signal (col. 10, lines 31-39). The claimed "demodulator coupled

to...the tuner, and to provide a transport stream" is met by digital demodulator 412, which provides the digital MPEG transport stream signals (col. 10, lines 37-44 and 51-56). The claimed ""video graphics adapter" having an input to receive the compressed transport stream" is met by the video graphics adapter (VGA) card 318, as shown in Fig. 5, where the controller 510 receives the MPEG encoded video stream (col. 11, lines 34-37). The claimed "video graphics adapter further includes a bus interface port coupleable to a central processing unit" is met by the PCI bus interface port from controller 510 in VGA card 318 (see Fig. 5 and col. 11, lines 35-38), which is coupleable to processor 310 via the PCI Bus (see Fig. 3 and col. 9, lines 17-24). The claimed VGA further includes an engine operative to decompress the compressed transport stream is met by the MPEG-2 decoder 512 in Fig. 5, which decompresses the MPEG transport stream (see col. 11, lines 37-44), and the claimed video output port is met by either the audio video output connector 542 (see col. 11, lines 61-63 and col. 12, lines 3-6), or the video output 522 as shown in Fig. 5 (see col. 11, lines 40-55, more specifically lines 52-55).

As to claim 19, the claimed VGA includes a memory to store at least a portion of the compressed transport stream is met by DRAM 514 in Fig. 5 (see col. 11, lines 37-47).

As to claim 20, the claimed central processor unit coupled to the bus interface port of the video graphics adapter is met by processor 310 (see Fig. 3 and col. 9, lines 17-24), which is coupled to the bus interface port (controller 510) of the VGA card 318 via the PCI BUS 312 (see Fig. 5 and col. 11, lines 35-38). The claimed transport demultiplexer coupled to the demodulator is met by the demultiplexer 416, which is coupled to the demodulator 412 through the F.E.C. 414 as shown in Fig. 4 (see col. 10, lines 40-58).

Assuming that claim 18 was intended to imply that the demodulator provide a compressed transport stream directly to the video graphics adapter, instead of the compressed transport stream being transmitted through the PCI bus to the video graphics adapter, the claims are also rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (USPN 5,900,867), as described in the rejection below.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheney et al (USPN 6,519,283), in view of Adams et al (USPN 6,108,042), both cited by the Examiner.

As to claim 14, note the Cheney et al reference which discloses a method of receiving video graphics data. The claimed "receiving a compressed transport stream associated with a digital video broadcast signal" is met by the digital video from cable or satellite broadcast signal 101 (Fig. 4) received at NIM 102, where a MPEG transport stream is sent to transport logic (XPORT) 103 (see col. 6, line 35-45). The MPEG transport stream is a compressed transport stream. In addition, the claimed "compressed transport stream having data signals and control signals" is inherent to a MPEG transport stream. The Applicants also disclose this in the "Background of the Invention" (or prior art) section of the specification, which describes the Digital Video Broadcast (DVB) transmission standards and specifically states that, "The

compressed MPEG 2 format is referred to as a transport stream. The transport stream from the demodulator comprises a plurality of packets. Each of the transport steam packets comprises one synchronization byte, followed by one of 187 data bytes or 187 data bytes plus 16 extra bytes depending on the format." (See Specification, page 1, lines 15-19). Therefore, it is well known in the art that a MPEG transport stream comprises data signals as met by the data byes, and control signals as met by the synchronization bytes. The claimed "generating a secondary set of control signals from the compressed transport stream's control signals" is met by the video decode system of Figure 6, where the MPEG input source if fed through the memory control unit 652 as coded MPEG 2 video data to the input of video decoder 654 and from the decoded signals from the MPEG transport stream's control signals, the frame buffer pointer control 686 generates additional control signals (see col. 9, line 31 – col. 10, line 41). The claimed "storing at least a portion of the compressed transport stream data signals in a memory buffer controlled by the secondary set of control signals" is met by the frame buffer pointer control 686 controlling the rotation of the frame buffers (see col. 10, lines 37-41). Although the Cheney reference discloses a PCI bus 42 (Fig. 2), the Cheney reference does not explicitly disclose the claimed sending the contents of the memory buffer to a system bus. The Adams et al reference teaches a Graphics Display Subsystem 56 in Fig. 2, which includes a frame buffer (col. 5, lines 41-43) that may send information to the system bus 51. Although the Adams reference teaches that the graphics display subsystem 56 is used primarily to drive the display device 12 (col. 5, lines 41-43), the Adams reference does not **only** teach a "method of sending the contents of a memory buffer in the direction of the display and not in the direction of the system bus," but also teaches that the relationship relating to communications between the Graphics Display Subsystem 56 and the

system bus 52 is bi-directional as shown in Fig. 2, where information may be communicated to other parts of the computer system, such as, the processor 52, memory subsystem 54, data modem 58, disk drive 60, etc. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the method of receiving video graphics data as disclosed by the Cheney et al reference with the teachings the Adams et al reference which discloses using a system bus in conjunction with the frame buffer memory for the advantage of having the ability to receive various types of television broadcasts through a computer system with a video graphics adapter and bus type system. One of ordinary skill in the art would have been led to make such a modification since television receivers used with computers are well known in the art to provide additional capabilities within a computer system.

As to claim 15, the Cheney reference discloses multiple modes of operation and a method of receiving a digital video signal that is of a different type than the compressed transport stream, which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67). The Cheney reference discloses a first mode of operation as shown by receiving a digital video signal 101, which includes a compressed MPEG transport stream (col. 6, lines 37-44). The Cheney reference also discloses another mode of operation wherein the digital video signal is of a different type than the compressed transport stream, which is met by the uncompressed digital video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col. 6, lines 62-67), which includes data signals including pixel data signals and control signals which are met by the corresponding synchronization signals (col. 4, lines 56-57), and by "pixel select control" signals (col. 7, lines 40-41). The digital multi-standard decoder (DMSD) 105 provides synchronization signals, such as, horizontal sync and vertical sync and the DMSD 105 provides

the synchronization signals to the video decoder 106 which interprets the synchronization information and processes the data (col. 7, lines 7-18) to provide a secondary set of control signals through the use of the frame buffer pointer control 686 and other circuitry as shown in the video decode system of Fig. 6 and as previously described above in claim 14.

As to claim 16, the Cheney reference as combined above, further discloses a camcorder or television camera may be used as an uncompressed signal and connected video cameras may inherently comprise the transmission of a zoom video signal (see col. 8, lines 24-25 and ZV port definition from the Microsoft Computer Dictionary, p. 586).

As to claim 17, the Cheney et al reference also discloses a method wherein the memory buffer is a frame buffer as shown in Fig. 2, DRAM 53 (col. 5, lines 65-67) and Fig. 6, element 653.

7. Claims 18-20 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (USPN 5,900,867).

As to claim 18, the Schindler et al reference discloses a system for receiving a digital video broadcast signal. The claimed "tuner to receive a digital broadcast signal and to provide an analog output signal" is met by tuner 410 in Fig. 4, which receives a digital signal that is transmitted on an analog carrier signal (col. 10, lines 31-39). The claimed "demodulator coupled to...the tuner, and to provide a transport stream" is met by digital demodulator 412, which provides the digital MPEG transport stream signals (col. 10, lines 37-44 and 51-56). The claimed ""video graphics adapter" having an input to receive the compressed transport stream" is met by the video graphics adapter (VGA) card 318, as shown in Fig. 5, where the controller 510

receives the MPEG encoded video stream (col. 11, lines 34-37). The claimed "video graphics adapter further includes a bus interface port coupleable to a central processing unit" is met by the PCI bus interface port from controller 510 in VGA card 318 (see Fig. 5 and col. 11, lines 35-38), which is coupleable to processor 310 via the PCI Bus (see Fig. 3 and col. 9, lines 17-24). The claimed VGA further includes an engine operative to decompress the compressed transport stream is met by the MPEG-2 decoder 512 in Fig. 5, which decompresses the MPEG transport stream (see col. 11, lines 37-44), and the claimed video output port is met by either the audio video output connector 542 (see col. 11, lines 61-63 and col. 12, lines 3-6), or the video output 522 as shown in Fig. 5 (see col. 11, lines 40-55, more specifically lines 52-55). Although, the Schindler et al reference teaches that the digital video broadcast signal as described above is transmitted through the PCI bus 312. Schindler also teaches that the VGA card 318 as shown in Fig. 5 may also directly receive broadcast signals through audio video inputs 524, 544, 546 and 548 (col. 11, lines 56-66), more specifically standard cable connector 524, which may receive broadcasts, is coupled to tuner circuit 526 (col. 11, lines 56-60), although the Schindler et al reference does not explicitly disclose that the video broadcast received through connector 524 is a digital video broadcast, the Examiner takes Official Notice that it would have been obvious to one of ordinary skill in the art to have modified the system of receiving a digital video broadcast signal of Schindler et al to include the tuner and demodulator circuitry for digital broadcasts, as disclosed in Fig. 4, to be directly connected to the VGA card 318 for the advantage of reducing hardware components, simplifying the system and bypassing the PCI bus, which would cut manufacturing costs and improve processing speed. Therefore, it is submitted that it would have been clearly obvious to one of ordinary skill in the art at the time of the invention to have the

tuner and demodulator circuitry for digital broadcasts directly connected to the video graphics adapter for the advantages given above.

As to claim 19, the claimed VGA includes a memory to store at least a portion of the compressed transport stream is met by DRAM 514 in Fig. 5 (see col. 11, lines 37-47).

As to claim 20, the claimed central processor unit coupled to the bus interface port of the video graphics adapter is met by processor 310 (see Fig. 3 and col. 9, lines 17-24), which is coupled to the bus interface port (controller 510) of the VGA card 318 via the PCI BUS 312 (see Fig. 5 and col. 11, lines 35-38). The claimed transport demultiplexer coupled to the demodulator is met by the demultiplexer 416, which is coupled to the demodulator 412 through the F.E.C. 414 as shown in Fig. 4 (see col. 10, lines 40-58).

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (USPN 5,900,867), in view of Malladi et al (USPN 5,912,676), and in further view of Datari (USPN 6,418,169), all cited by the Examiner.

As to claim 21, note the Schindler et al reference which discloses a method of storing video data. Schindler et al discloses multiple modes of operation, such as receiving a digital video broadcast signal from a satellite dish as shown in Fig. 4, or receiving a standard cable broadcast signal at 524 as shown in Fig. 5. The claimed first mode of operation comprising storing pixel information in a frame buffer of a video adapter, wherein one line of frame buffer memory is representative of one line of a video image to be displayed is met in part by receiving an uncompressed signal from a cable video source through connector 524 (Fig. 5), as described above, where the video signal may be buffered in VRAM 518 for output to a monitor (see col.

11, line 56 – col. 12, line 3). Although, Schindler does not explicitly disclose that one line of the frame buffer memory is representative of a line of video image to be displayed, it is well known in the art of uncompressed video frame buffers that a line of frame buffer memory may be *representative* of a line of a video image to be displayed. The Malladi et al reference teaches that various frame storage formats exist for storing frame data in memory, and that one method for storing a frame of pixel data is on a scan line basis, where the data is stored in memory scan line by scan line for pictures or frames that are to be displayed (see col. 4, lines 30-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the method of the Schindler et al reference which discloses multiple modes of operation and storing video data, with the Malladi et al reference, which specifically teaches that one line of frame buffer memory may be representative of one line of a video image to be displayed for the advantage of providing a storage format which provides improved performance for storing a reference frame of pixel data on a scan line basis. The claimed second mode of operation comprising storing compressed transport stream data in the frame buffer, wherein one line of frame buffer memory is representative of one transport stream packet is met in part by the Schindler et al reference, which also discloses receiving an MPEG transport stream from a digital video source Fig 4, as described above, where the compressed MPEG transport stream is sent to the PCI bus 312, where the video graphics adapter card receives the MPEG stream through controller 510 (Fig. 5, col. 11, lines 34-37), and the MPEG data is routed to MPEG-2 decoder 512 with associated random access memory (DRAM 514), which is used as a frame buffer where the video is decoded (col. 11, lines 37-47) and eventually sent to a display. Although, the Schindler et al reference does not explicitly disclose that one line of the frame

buffer memory is representative of one transport stream packet, it is well known in the art of video transport streams that are stored in frame buffers that a MPEG-2 transport stream packet has a fixed 188 byte length as defined by MPEG standards, and therefore, a line of frame buffer memory is *representative* of a transport stream packet since every MPEG-2 transport stream packet has already been produced and transmitted according to the established MPEG standards so that when received by a frame buffer memory a line of memory is representative of one transport stream packet. In addition to, the Datari reference teaches that MPEG video data packets may be stored or buffered in memory and sequentially accessed by priority (see col. 5, lines 13-42 and col. 6, lines 62-66, also see col. 8, lines 10-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further combined the method of Schindler et al which discloses multiple modes of operation and storing video data, with the Datari reference, which specifically teaches that a line of the frame buffer memory may be representative of one MPEG or transport stream packet for the advantage of providing a storage format which allows for improved priority accessing of transport stream packets of video images to be displayed.

Allowable Subject Matter

9. Claims 2-13 and 22-23 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 22, the prior art, alone or in combination, does not teach or fairly suggest a video graphics system comprising a data storage controller having at least one pair of a plurality of internal control ports to communicate control signals within the data storage controller.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael W. Hoye whose telephone number is (703) 305-6954. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at (703) 305-4795.

Any response to this action should be mailed to:

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is **(703) 308-HELP**.

Michael W. Hoye
July 12, 2004

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600